REMARKS

Claims 1-15 and 23-37 are pending in the action, with claims 1 and 23 being independent.

Claims 1-3, 5-6, 11-15, 23-25, 27-28 and 33-37 are rejected under 35 U.S.C. §102(b) as being anticipated by USP No. 5,964,856 to **Wu**.

Claims 4 and 26 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over **Wu** in view of USP No. 5,732,249 to **Masuda**.

Claims 7 and 29 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over **Wu** in view of USP No. 5,355,468 to **McDaniel**.

Claims 8-10 and 30-32 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Wu in view of USP No. 5,355,468 to **Jeppesen**.

Applicant respectfully traverses these rejections. Reconsideration and allowance of the above-referenced application are respectfully requested in light of the following comments and remarks.

Section 102(b) Rejections

Claims 1-3, 5-6, 11-15, 23-25, 27-28 and 33-37 are rejected as being anticipated by Wu. Applicant respectfully traverses these rejections.

Claim 1 recites in part a driver in communication with a clock bus, the driver to drive and maintain a voltage of the **clock bus** to a first voltage level.

In the statement of rejection, the Examiner alleges that Wu's strobe signal STB_p drives a clock bus to a first voltage during the period from 4A to 4B. *See*, page 2, item 3, lines 1-9 of Office Action. Applicant respectfully disagrees with this finding, as Wu explicitly states that the STB_p strobe signal is used to drive data onto the "DATA" bus, **not** the clock bus, which enables Wu to synchronize the transfer of data and latch data when needed (5:22-25 and 5:56-58).

Further, claim 1 recites that the driver drives and maintains the voltage of the clock bus to the first voltage level when a clock transmitter is not transmitting a clock signal on the clock bus

and a clock receiver is not receiving a clock signal on the clock bus. Applicant respectfully asserts that Wu does not teach or suggest such a driver.

The Examiner reads Wu's "two-dead-clocks period" as a period in which neither Wu's clock transmitter transmit nor clock receiver receive clock signals. *See*, page 2, item 3, lines 5-10 of Office Action. Applicant respectfully disagrees. Applicant respectfully submits that during Wu's "two-dead-clocks period" (i.e., from period 3B to period 5A), Wu's microprocessor continues to output the clock signals INTCLK (clock internal to the processor) and BCLK (clock as seen on the bus). Wu's objective in outputting the clock signals during the "two-dead-clocks period" is to effectuate data clocking (5:9-14 & 6:4-9) and to provide a clock cycle sufficient to allow Wu's processor requesting the use of a DATA bus to become the bus master (5:56-67).

For at least the foregoing reasons, Applicant respectfully submits that Wu does not anticipate claim 1. Claims 2-3, 5-6 and 11-15, depend from claim 1, and also are submitted to be allowable for at least the reasons discussed with respect to claim 1.

Claim 23

Claim 23 recites in part a voltage driving means for driving and maintaining a voltage of the clock bus to a first voltage level while the clock signal transmission means is not transmitting a clock signal on the clock bus and the clock signal receiving means is not receiving a clock signal on the clock bus.

As discussed above, Wu does not teach or suggest at least this feature. For at least these reasons, Applicant respectfully submits that Wu does not anticipate claim 23. Claims 24-25, 27-28 and 33-37 depend from claim 8, and also are submitted to be allowable for at least the reasons discussed above with respect to claim 8.

Section 103(a) Rejections

Claims 4 and 26 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Wu in view of Masuda.

Claim 4 depends from claim 1, and also is submitted to be allowable for at least the reasons discussed above with respect to claim 1.

Claim 26 depends from claim 23, and also is submitted to be allowable for at least the reasons discussed above with respect to claim 23.

Section 103(a) Rejections

Claims 7 and 29 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Wu in view of USP No. 5,355,468 to McDaniel.

Claim 7 depends from claim 1, and also is submitted to be allowable for at least the reasons discussed above with respect to claim 1.

Claim 29 depends from claim 23, and also is submitted to be allowable for at least the reasons discussed above with respect to claim 23.

Section 103(a) Rejections

Claims 8-10 and 30-32 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Wu in view of Jeppesen.

Claim 8-10 depend from claim 1, and also are submitted to be allowable for at least the reasons discussed above with respect to claim 1.

Claims 30-32 depend from claim 23, and also are submitted to be allowable for at least the reasons discussed above with respect to claim 23.

Conclusion

Applicant respectfully requests that all pending claims be allowed over the prior art of record.

By responding in the foregoing remarks only to particular positions taken by the Examiner, Applicant does not acquiesce with other positions that have not been explicitly addressed. In addition, Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

For all of the reasons set forth above, Applicant respectfully submits that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's undersigned at the telephone number shown below.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 06-1050 and please credit any excess fees to such deposit account.

Respectfully submitted,

Date: March 12, 2008

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